and FETs **104a**, **104b**, a void **116** develops as a result of the narrow spacing between FETs **104a**, **104b**.

A1

Page 8 lines 9-17:

Fig. 3 shows a portion of a partially processed wafer having gate electrodes **106** disposed over gate dielectric layers **107**, with gate dielectric layers **107** disposed, in turn, on the surface of a substrate **102**. Tip regions (sometimes referred to as source/drain extensions) **302** are disposed in substrate **102** in alignment with gate electrodes **106**. [This] Those skilled in this field will recognize that these tip regions are generally formed by ion implantation, and that the material implanted is of a conductivity type opposite the conductivity type of substrate **102**. Gate electrodes **106**, gate dielectrics **107**, and tip regions **302**, may be formed by conventional well-known methods.

A2

Claim Rejections - 35 U.S.C. § 103

Claims 1-14, 16 and 17 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Chern et al. (U.S. Patent No. 6,150,223) in view of Laxman et al. (U.S. Patent No. 5,976,991). In rejecting these claims, the Office Actions states, on p. 3 line 20 - p. 4 line 4:

Thus, Chern is shown to teach all the features of the claim with the exception of using a specific precursor silane.

However, Laxman teaches an alternative silane precursor such as bis-(tertiarybutylamino)silane (BTBAS) can be used to form silicon oxide and silicon nitride. Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to form the silicon oxide (20s), silicon nitride (22s) and silicon oxide (24s) of Chern using BTBAS as taught by Laxman to avoid Si-C bonds to reduce carbon contamination of the resulting films.

Applicants respectfully submit, however, that this conclusion of obviousness is improperly drawn in hindsight only after reading Applicant's claims. The Office Action does not point out any teaching or suggestion from Chern or Laxman as to why one of ordinary skill in the art would have been motivated to combine the teachings in the manner suggested in the Office Action, other than to reduce carbon contamination of the resulting films, which is the stated reason for Laxman's invention. Chern does not present carbon contamination as a problem and makes no suggestion of using a method that might reduce carbon contamination.

Applicants also submit that while Laxman teaches, in column 5, line 64 to column 6, that BTBAS may be used to form dielectric layers of varying concentrations of oxygen and nitrogen, the details are vague with respect to forming layers of silicon nitride. Further, Applicants submit that Laxman provides no details as to a specific sequence of types of layers (i.e. silicon oxide, silicon nitride, silicon oxide) as claimed in independent claims 1 and 11 of the present application.

Accordingly, Applicants submit that both references lack the required suggestion or motivation to combine the references, as suggested in the Office Action. Accordingly, Applicants submit that independent claims 1 and 11 are patentable over Chern in view of Laxman. Claims 2-14, 16 and 17 each depend, directly or indirectly, from claims 1 and 11. Therefore, Applicant submits that claims 2-14, 16 and 17 are also patentable over Chern in view of Laxman. Accordingly, Applicant respectfully requests the rejection be withdrawn.

With respect to claims 7 and 9, the Examiner has also taken Official Notice that purging the furnace prior to forming different films is within the ability of one having ordinary skill in the art. With respect to claims 8 and 10, the Examiner has taken Official Notice that how purging is performed is also within the ability of one having ordinary skill in the art. However, Applicants